Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.098”**

**.095”**

**OUT**

**IN**

**IN**

**OUT**

**GND**

**1**

**2**

**3**

**F**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 123F**

**APPROVED BY: DK DIE SIZE .095” X .098” DATE: 7/11/22**

**MFG: NATIONAL THICKNESS .010” P/N: LM123**

**DG 10.1.2**

#### Rev B, 7/1